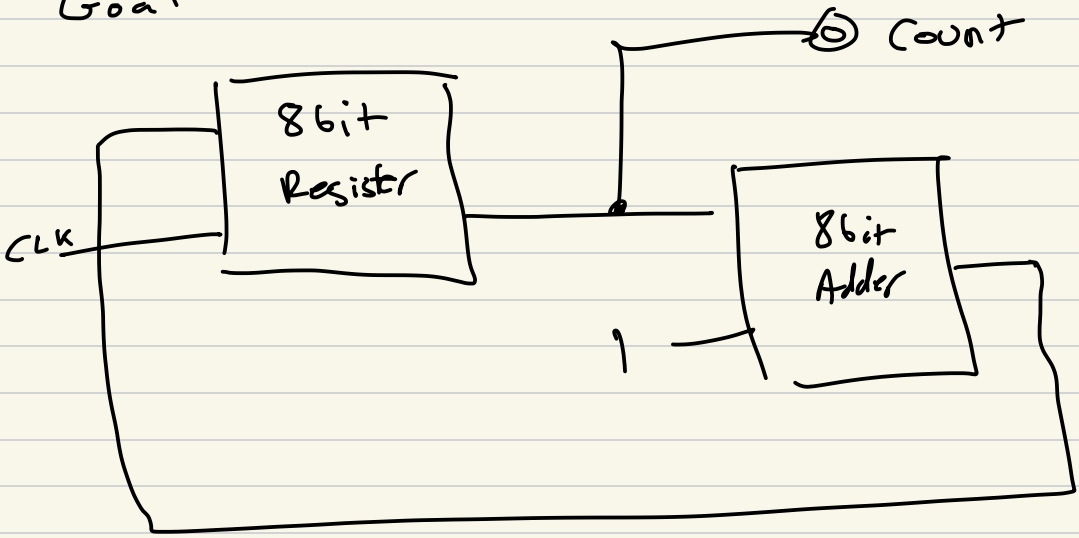
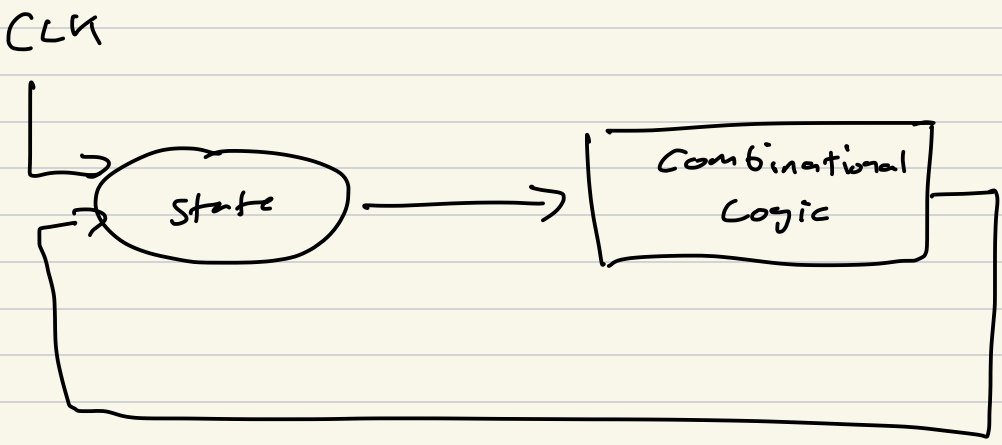
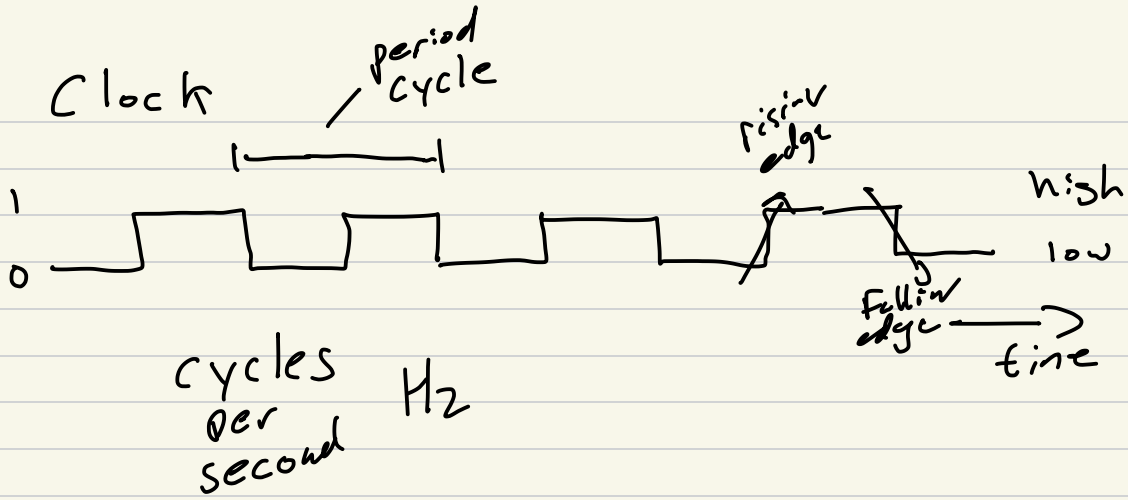
CS315-02 Lab Sequential Logic

Goal

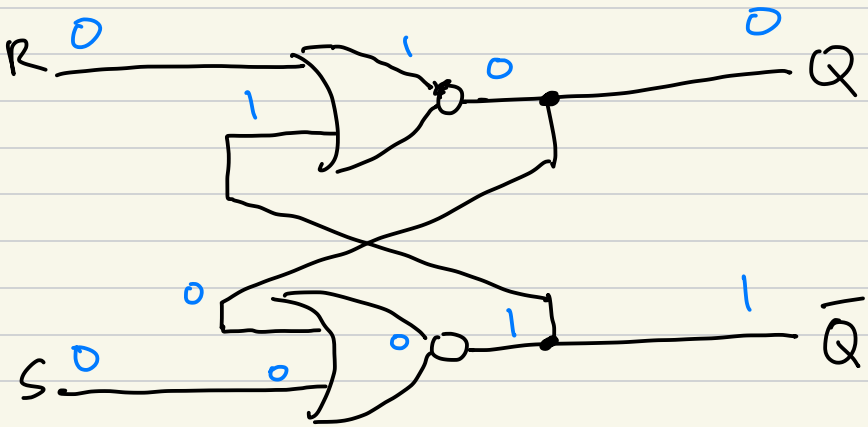


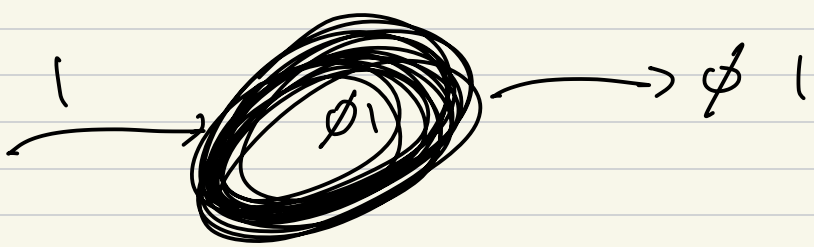


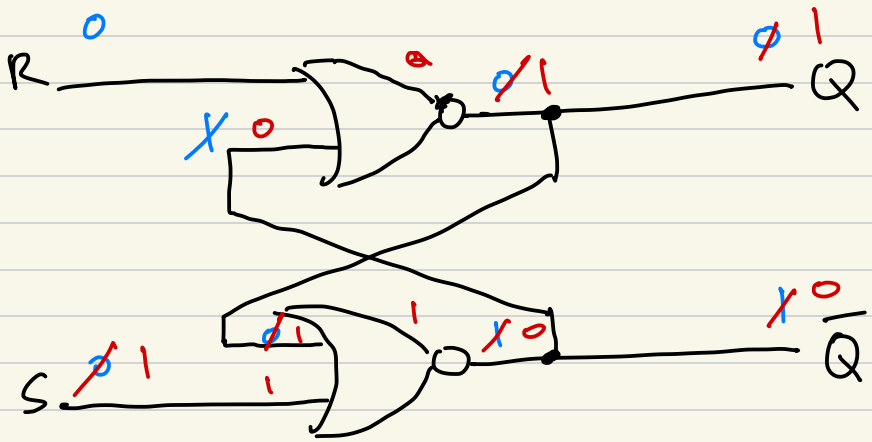


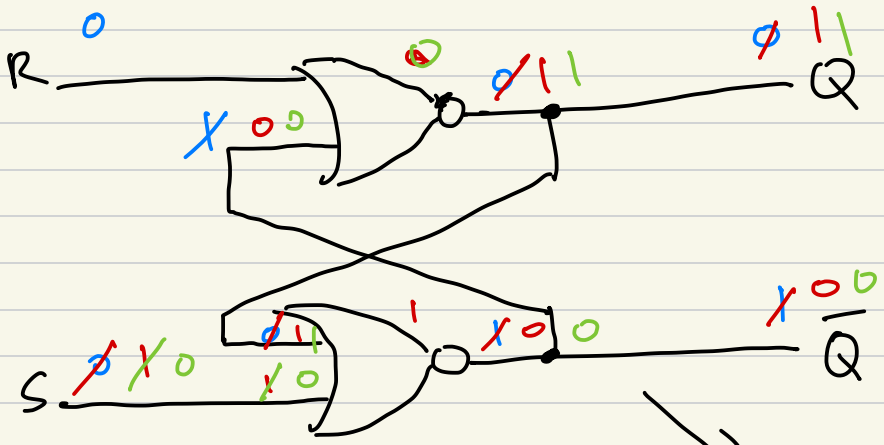
How to store a 1 bit value?

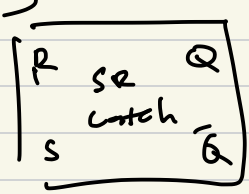
SR Latch set reset











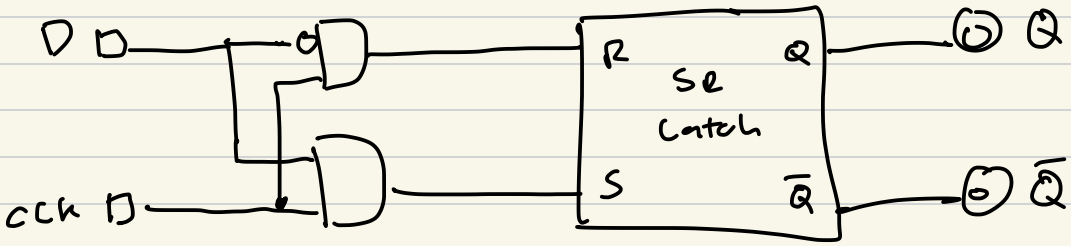
time ↓

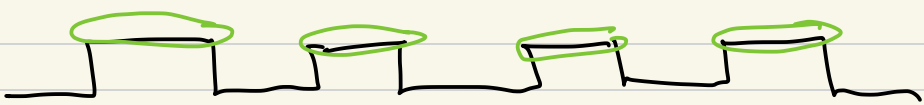
R	S	Q	$\bar{Q}$
0	0	0	1
0	1	1	0
0	0	1	0
1	0	0	1
0	0	0	1
1	1	X	X

undefined

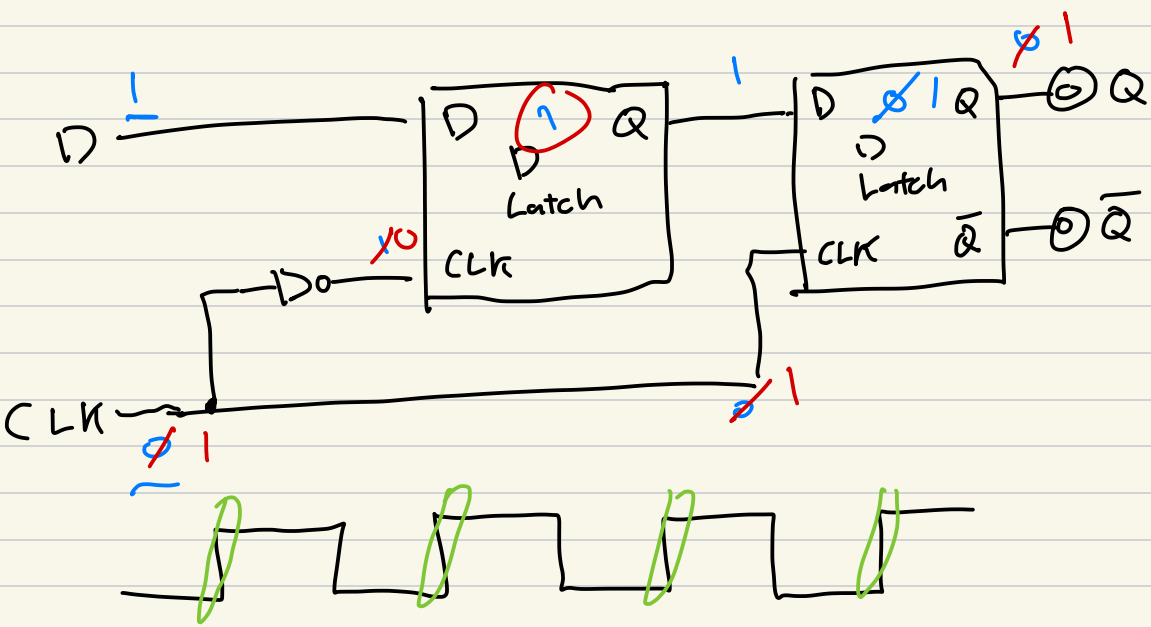
SR Latch → D flip-flop → 1 bit register → N bit register → counter

D Latch



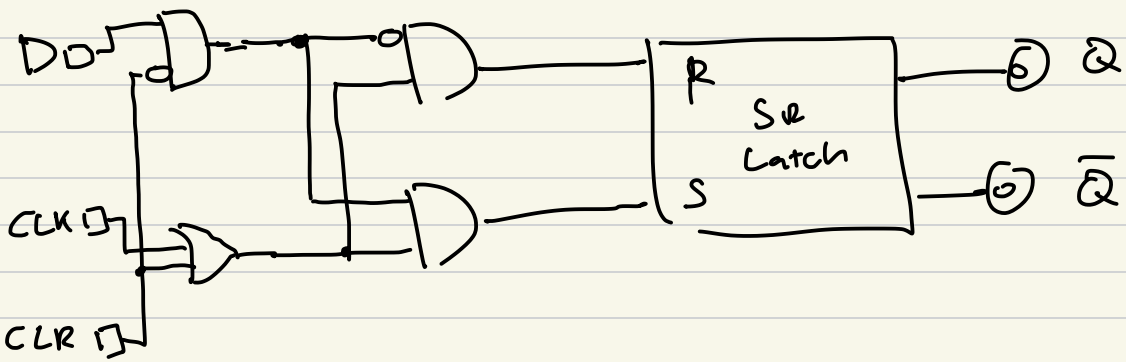


D Flip-Flop

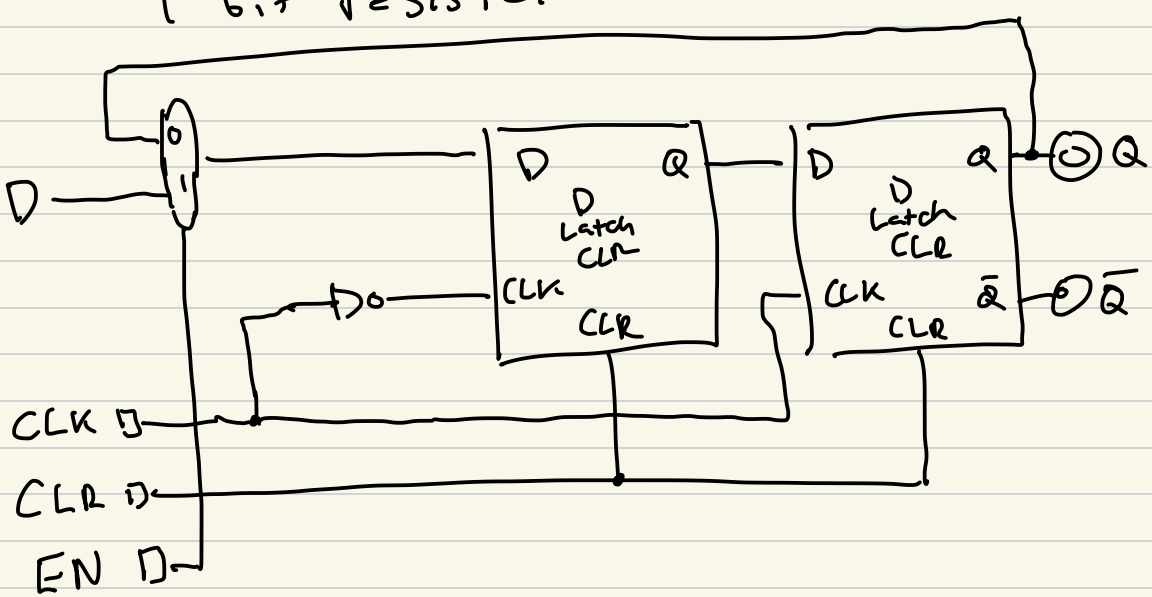


1 bit resister

D Latch with CLR



1 bit resister CLR + EN



4 bit register